

SN74AHC1G08 Single 2-Input Positive-AND Gate

1 Features

- Operating Range 2 V to 5.5 V
- Maximum t_{pd} of 7 ns at 5 V
- Low Power Consumption, 10- μ A Maximum I_{CC}
- ± 8 -mA Output Drive at 5 V
- Schmitt-Trigger Action at All Inputs Makes the Circuit Tolerant for Slower Input Rise and Fall Time
- Latch-Up Performance Exceeds 250 mA Per JESD 17

2 Applications

- Barcode Scanners
- Cable Solutions
- E-Books
- Embedded PCs
- Field Transmitter: Temperature or Pressure Sensors
- Fingerprint Biometrics
- HVAC: Heating, Ventilating, and Air Conditioning
- Network-Attached Storage (NAS)
- Server Motherboard and PSU
- Software Defined Radios (SDR)
- TV: High Definition (HDTV), LCD, and Digital
- Video Communications Systems
- Wireless Data Access Cards, Headsets, Keyboards, Mice, and LAN Cards

3 Description

The SN74AHC1G08 device is a single 2-input positive-AND gate. The device performs the Boolean function $Y = A \bullet B$ or $Y = \overline{A} + \overline{B}$ in positive logic.

Package Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE ⁽²⁾	BODY SIZE ⁽³⁾
SN74AHC1G08	DBV (SOT-23, 5)	2.9 mm x 2.8 mm	2.9 mm x 1.6 mm
	DCK (SC-70, 5)	2 mm x 2.1 mm	2 mm x 1.25 mm
	DRL (SOT, 5)	1.6 mm x 1.6 mm	1.6 mm x 1.2 mm

- (1) For all available packages, see the orderable addendum at the end of the data sheet.
- (2) The package size (length x width) is a nominal value and includes pins, where applicable.
- (3) The body size (length x width) is a nominal value and does not include pins.



Logic Diagram (Positive Logic)



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4 Pin Configuration and Functions

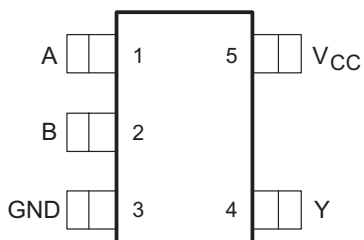


Figure 4-1. DBV Package 5-Pin SOT-23 Top View

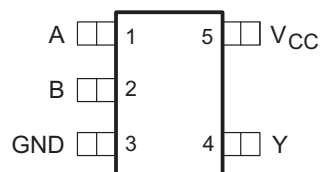
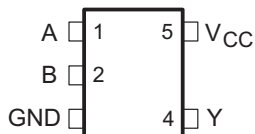


Figure 4-2. DCK Package 5-Pin SC70 Top View



See mechanical drawings for dimensions (in [Section 11](#)).

Figure 4-3. DRL Package 5-Pin SOT Top View

Table 4-1. Pin Functions

PIN		TYPE ⁽¹⁾	DESCRIPTION
NO.	NAME		
1	A	I	Data Input
2	B	I	Data Input
3	GND	—	Ground
4	Y	O	Data Output
5	VCC	—	Power

(1) Signal Types: I = Input, O = Output, I/O = Input or Output

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V_{CC}	Supply voltage	−0.5	7	V
V_I	Input voltage ⁽²⁾	−0.5	7	V
V_O	Output voltage ⁽²⁾	−0.5	$V_{CC} + 0.5$	V
I_{IK}	Input clamp current	$V_I < 0$		−20 mA
I_{OK}	Output clamp current	$V_O < 0$ or $V_O > V_{CC}$		±20 mA
I_O	Continuous output current	$V_O = 0$ to V_{CC}		±25 mA
	Continuous current through V_{CC} or GND			±50 mA
T_J	Junction temperature			150 °C
T_{stg}	Storage temperature	−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	±2000
		Charged-device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	±1000

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V_{CC}	Supply voltage	2	5.5	V
V_{IH}	High-level input voltage	$V_{CC} = 2\text{ V}$	1.5	V
		$V_{CC} = 3\text{ V}$	2.1	
		$V_{CC} = 5.5\text{ V}$	3.85	
V_{IL}	Low-level input voltage	$V_{CC} = 2\text{ V}$	0.5	V
		$V_{CC} = 3\text{ V}$	0.9	
		$V_{CC} = 5.5\text{ V}$	1.65	
V_I	Input voltage	0	5.5	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 2\text{ V}$	−50	μA
		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	−4	mA
		$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$	−8	
I_{OL}	Low-level output current	$V_{CC} = 2\text{ V}$	50	μA
		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	4	mA
		$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$	8	
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	100	ns/V
		$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$	20	

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

	MIN	MAX	UNIT
T _A Operating free-air temperature	–55	125	°C

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, [SCBA004](#).

5.4 Thermal Information

THERMAL METRIC ⁽¹⁾	SN74AHC1G08			UNIT
	DBV (SOT-23)	DCK (SC70)	DRL (SOT)	
	5 PINS	5 PINS	5 PINS	
R _{θJA} Junction-to-ambient thermal resistance	278	289.2	142	°C/W

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			T _A = –55°C to 125°C		UNIT
			MIN	TYP	MAX	MIN	MAX	
V _{OH} High level output voltage	I _{OH} = –50 μA	2 V	1.9	2		1.9		V
		3 V	2.9	3		2.9		
		4.5 V	4.4	4.5		4.4		
	I _{OH} = –4 mA	3 V	2.58			2.48		
	I _{OH} = –8 mA	4.5 V	3.94			3.8		
V _{OL} Low level output voltage	I _{OL} = 50 μA	2 V			0.1		0.1	V
		3 V			0.1		0.1	
		4.5 V			0.1		0.1	
	I _{OL} = 4 mA	3 V			0.36		0.44	
	I _{OL} = 8 mA	4.5 V			0.36		0.44	
I _I Input leakage current	V _I = 5.5 V or GND	0 V to 5.5 V			±0.1		±1	μA
I _{CC} Supply current	V _I = V _{CC} or GND, I _O = 0	5.5 V			1		10	μA
C _i Input Capacitance	V _I = V _{CC} or GND	5 V		4	10		10	pF

5.6 Switching Characteristics, V_{CC} = 3.3 V ± 0.3 V

over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	T _A = 25°C			T _A = –40°C to 85°C		T _A = –55°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	A or B	Y	C _L = 15 pF		6.2	8.8	1	10.5	1	11	ns
t _{PHL}					6.2	8.8	1	10.5	1	11	
t _{PLH}	A or B	Y	C _L = 50 pF		8.7	12.3	1	14	1	14.5	ns
t _{PHL}					8.7	12.3	1	14	1	14.5	

5.7 Switching Characteristics, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$

over recommended operating free-air temperature range, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C to } 85^\circ\text{C}$		$T_A = -55^\circ\text{C to } 125^\circ\text{C}$		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	$C_L = 15\text{ pF}$		4.3	5.9	1	7	1	7.5	ns
t_{PHL}					4.3	5.9	1	7	1	7.5	
t_{PLH}	A or B	Y	$C_L = 50\text{ pF}$		5.8	7.9	1	9	1	9.5	ns
t_{PHL}					5.8	7.9	1	9	1	9.5	

5.8 Operating Characteristics

$V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load, $f = 1\text{ MHz}$	18	pF

5.9 Typical Characteristics

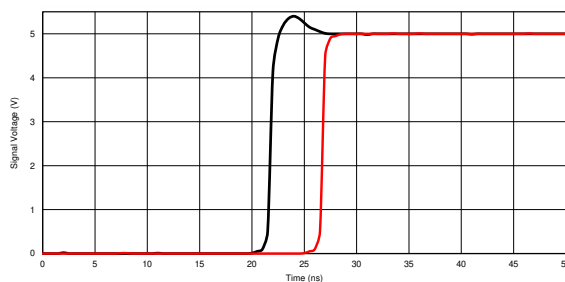
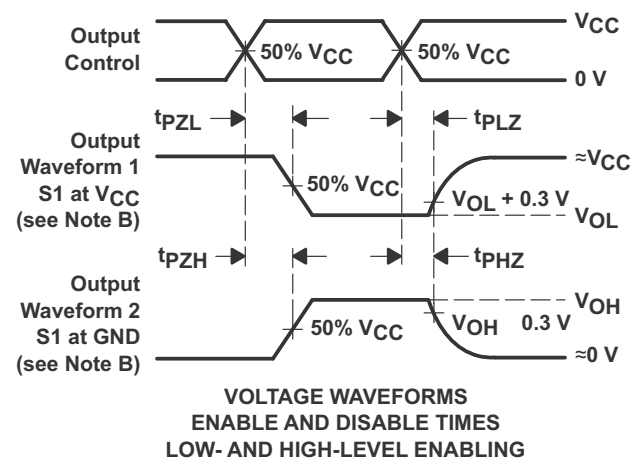
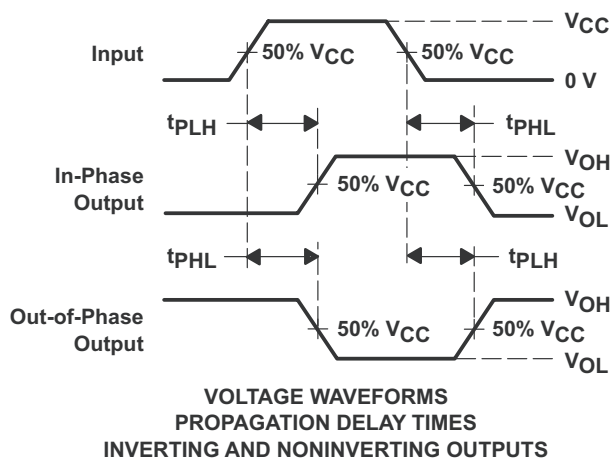
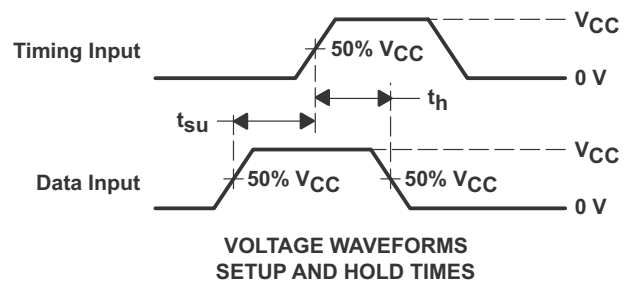
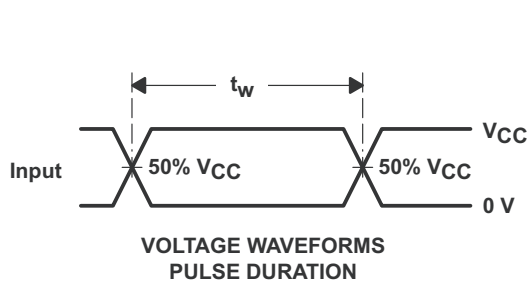
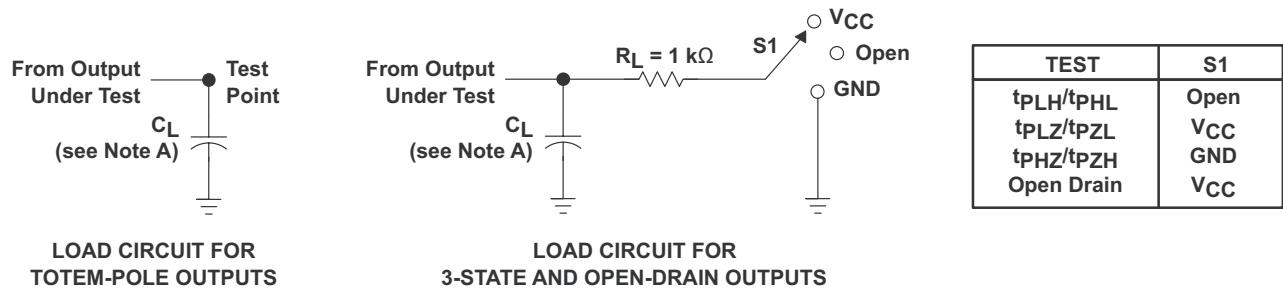


Figure 5-1. Response Time vs Output Voltage ($T_A = 25^\circ\text{C}$, $V_A = 5\text{ V}$)

6 Parameter Measurement Information



- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\text{ }\Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
- D. The outputs are measured one at a time with one input transition per measurement.
- E. All parameters and waveforms are not applicable to all devices.

Figure 6-1. Load Circuit and Voltage Waveforms

7 Detailed Description

7.1 Overview

The SN74AHC1G08 device is a single 2-input positive-AND gate. The device performs the Boolean function $Y = A \bullet B$ or $Y = \overline{A + B}$ in positive logic.

7.2 Functional Block Diagram



Figure 7-1. Logic Diagram (Positive Side)

7.3 Feature Description

The SN74AHC1G08 device has a wide operating V_{CC} range of 2 V to 5.5 V, which allows it to be used in a broad range of systems. The low propagation delay allows fast switching and higher operation speeds. In addition, the low-power consumption makes this device a good choice for portable and battery power-sensitive applications.

7.4 Device Functional Modes

Table 7-1 lists the functional modes for SN74AHC1G08.

Table 7-1. Function Table

INPUTS ⁽¹⁾		OUTPUT ⁽²⁾
A	B	Y
H	H	H
L	X	L
X	L	L

(1) H = High Voltage Level, L = Low Voltage Level, X = Don't Care

(2) H = Driving High, L = Driving Low, Z = High Impedance State

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

A common application for AND gates is their use in power sequencing. Power sequencing is often employed in applications that require a processor or other delicate device with specific voltage timing requirements in order to protect the device from malfunctioning. Using the SN74AHC1G08 to verify that the processor has turned on can protect it from any harmful signals.

8.2 Typical Application

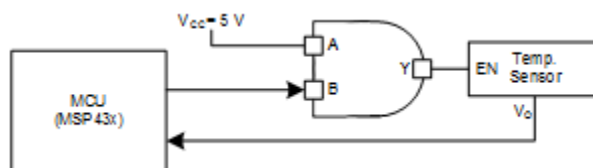


Figure 8-1. Power Sequencing Application

8.2.1 Design Requirements

The SN74AHC1G08 device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits.

The SN74AHC1G08 allows switching control of analog and digital signals with a digital control signal. All input signals should remain as close to either 0 V or V_{CC} as possible for optimal operation.

8.2.2 Detailed Design Procedure

- Recommended input conditions:
 - For rise time and fall time specifications, see $\Delta t/\Delta v$ in the [Section 5.3](#) table.
 - For specified high and low levels, see V_{IH} and V_{IL} in the [Section 5.3](#) table.
 - Inputs and outputs are overvoltage tolerant and can therefore go as high as 5.5 V at any valid V_{CC} .
- Recommended output conditions:
 - Load currents should not exceed ± 50 mA.
- Frequency selection criterion:
 - The effects of frequency upon the device's power consumption should be studied in *CMOS Power Consumption and CPD Calculation*, [SCAA035](#).
 - Added trace resistance and capacitance can reduce maximum frequency capability; follow the layout practices listed in the [Section 8.4](#) section.

8.2.3 Application Curves

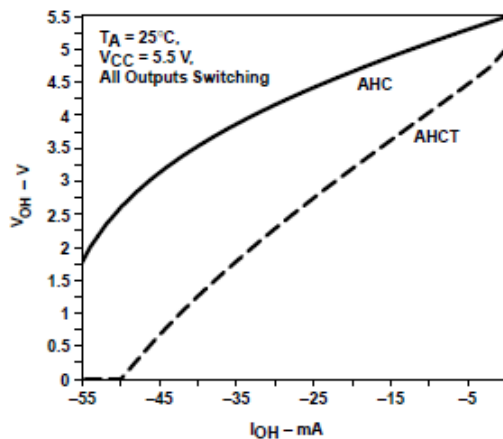


Figure 8-2. AHC Family V_{OH} vs I_{OH} at $V_{CC} = 5.5$ V

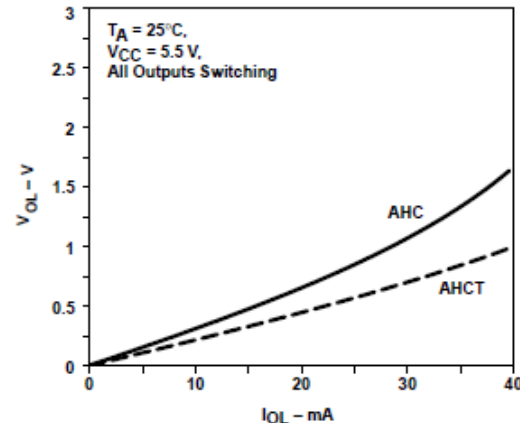


Figure 8-3. AHC Family V_{OL} vs I_{OL} at $V_{CC} = 5.5$ V

8.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating listed in the [Section 5.3](#) table.

Each V_{CC} terminal should have a bypass capacitor to prevent power disturbance. A 0.1- μ F bypass capacitor is recommended for devices with a single supply. If multiple pins are labeled V_{CC} , then a 0.01- μ F or 0.022- μ F capacitor is recommended for each V_{CC} because the V_{CC} pins are tied together internally. For devices with dual-supply pins operating at different voltages, for example V_{CC} and V_{DD} , a 0.1- μ F bypass capacitor is recommended for each supply pin. Use multiple bypass capacitors in parallel to reject different frequencies of noise. Capacitors with values of 0.1 μ F and 1 μ F are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

8.4 Layout

8.4.1 Layout Guidelines

Reflections and matching are closely related to the loop antenna theory but are different enough to be discussed separately from the theory. When a PCB trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self-inductance of the trace which results in the reflection. Not all PCB traces can be straight and therefore some traces must turn corners. [Figure 8-4](#) shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

8.4.1.1 Layout Example

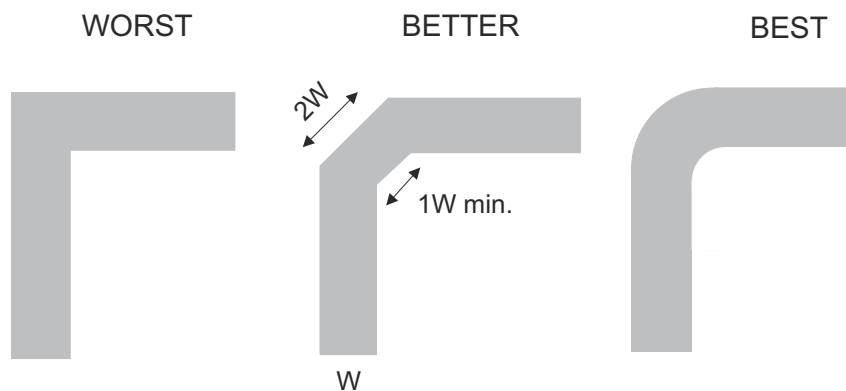


Figure 8-4. Trace Example

9 Device and Documentation Support

9.1 Documentation Support (Analog)

9.1.1 Related Documentation

For related documentation see the following:

- *Implications of Slow or Floating CMOS Inputs*, [SCBA004](#)
- *CMOS Power Consumption and CPD Calculation*, [SCAA035](#)
- *Selecting the Right Texas Instruments Signal Switch*, [SZZA030](#)

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

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9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision Q (October 2023) to Revision R (January 2024)	Page
• Updated RθJA values: DBV = 206 to 278, all values in °C/W	5

Changes from Revision P (March 2016) to Revision Q (October 2023)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document.....	1
• Updated RθJA values: DCK = 252 to 289.2, all values in °C/W	5

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74AHC1G08DBV3	Obsolete	Production	SOT-23 (DBV) 5	-	-	Call TI	Call TI	-55 to 125	A08Y
SN74AHC1G08DBVR	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-55 to 125	(38EH, 3BVF, A083, A08G, A08J, A08L, A08S)
SN74AHC1G08DBVR.A	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-55 to 125	(38EH, 3BVF, A083, A08G, A08J, A08L, A08S)
SN74AHC1G08DBVRE4	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	A08G
SN74AHC1G08DBVRG4	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	A08G
SN74AHC1G08DBVRG4.A	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	A08G
SN74AHC1G08DBVT	Obsolete	Production	SOT-23 (DBV) 5	-	-	Call TI	Call TI	-55 to 125	(A083, A08G, A08J, A08S)
SN74AHC1G08DBVTG4	Active	Production	SOT-23 (DBV) 5	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	A08G
SN74AHC1G08DBVTG4.A	Active	Production	SOT-23 (DBV) 5	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	A08G
SN74AHC1G08DCKR	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-55 to 125	(1B9, AE3, AEG, AEJ, AEL, AES)
SN74AHC1G08DCKR.A	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-55 to 125	(1B9, AE3, AEG, AEJ, AEL, AES)
SN74AHC1G08DCKRE4	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	AE3
SN74AHC1G08DCKRG4	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	AE3
SN74AHC1G08DCKRG4.A	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	AE3
SN74AHC1G08DCKT	Obsolete	Production	SC70 (DCK) 5	-	-	Call TI	Call TI	-55 to 125	(AE3, AEG, AEJ, AES)
SN74AHC1G08DCKTE4	Active	Production	SC70 (DCK) 5	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	AE3
SN74AHC1G08DCKTG4	Active	Production	SC70 (DCK) 5	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	AE3
SN74AHC1G08DCKTG4.A	Active	Production	SC70 (DCK) 5	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	AE3
SN74AHC1G08DRLR	Active	Production	SOT-5X3 (DRL) 5	4000 LARGE T&R	Yes	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-55 to 125	(AEB, AES)
SN74AHC1G08DRLR.A	Active	Production	SOT-5X3 (DRL) 5	4000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-55 to 125	(AEB, AES)
SN74AHC1G08DRLRG4	Active	Production	SOT-5X3 (DRL) 5	4000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-55 to 125	(AEB, AES)

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

(2) Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) RoHS values: Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF SN74AHC1G08 :

- Automotive : [SN74AHC1G08-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

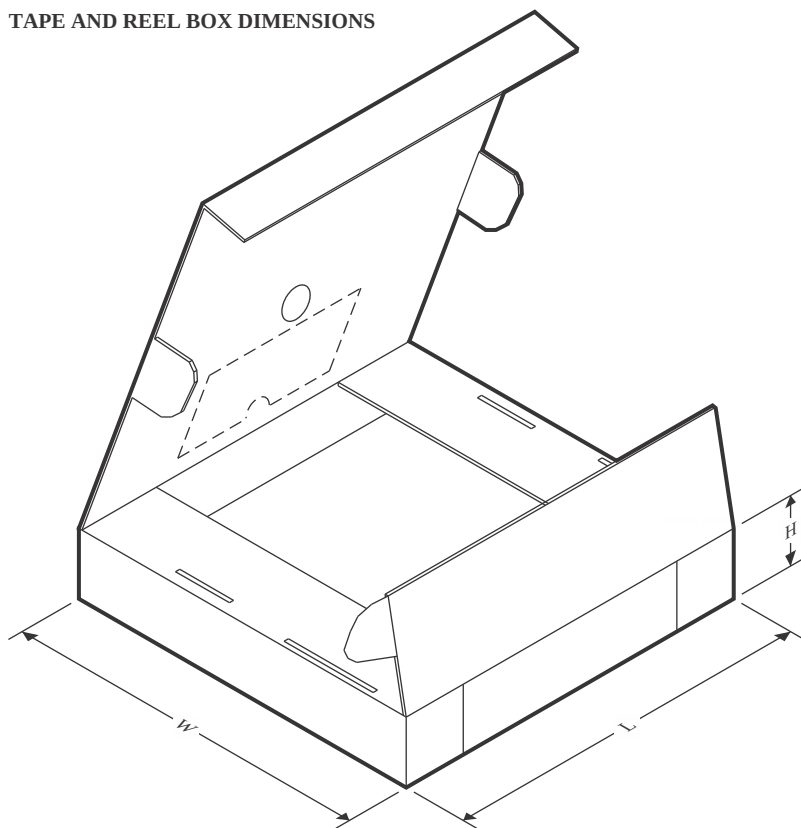
TAPE AND REEL INFORMATION



*All dimensions are nominal

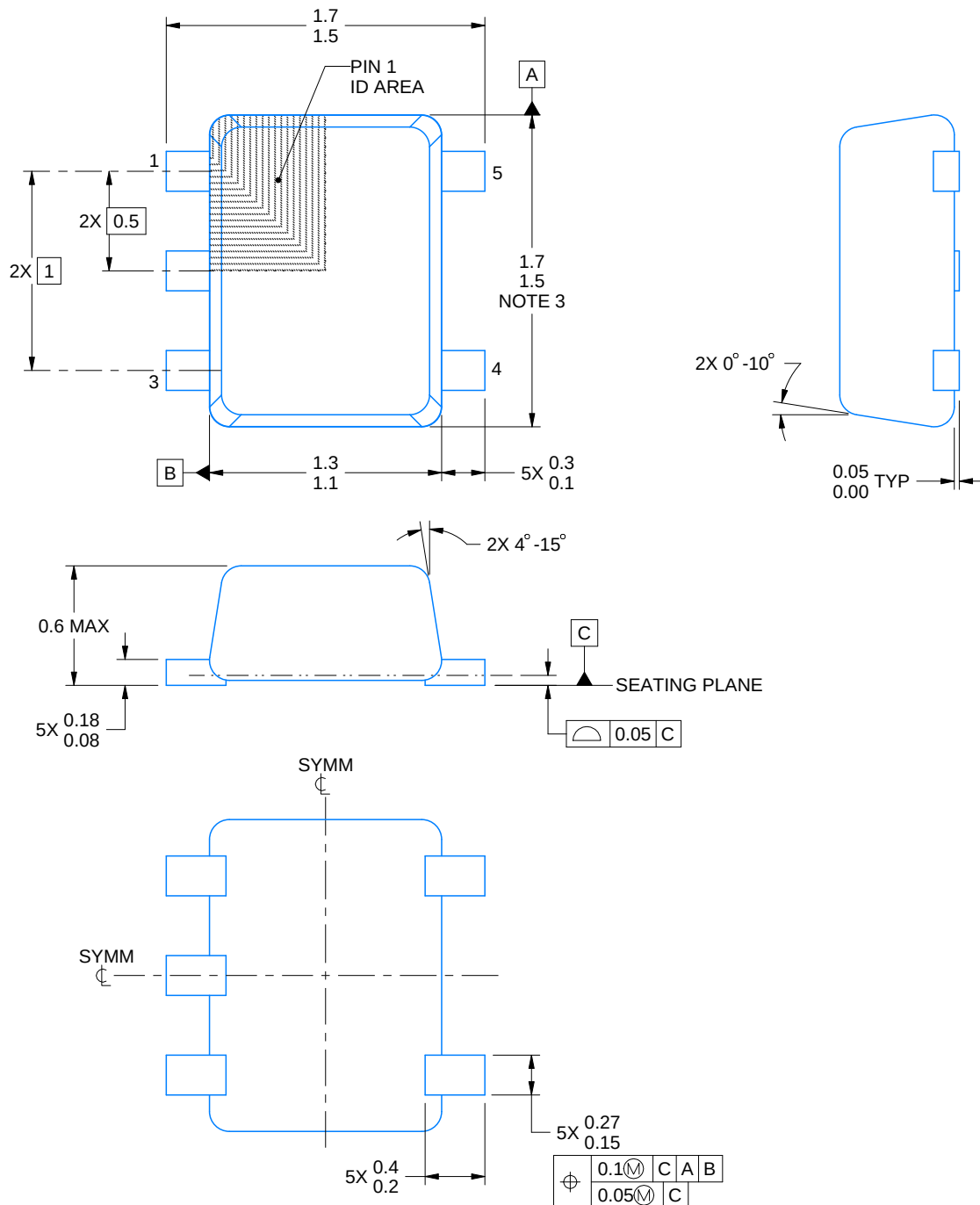
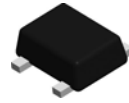
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHC1G08DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74AHC1G08DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74AHC1G08DBVRG4	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
SN74AHC1G08DBVTG4	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
SN74AHC1G08DCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74AHC1G08DCKR	SC70	DCK	5	3000	180.0	8.4	2.3	2.55	1.2	4.0	8.0	Q3
SN74AHC1G08DCKRG4	SC70	DCK	5	3000	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74AHC1G08DCKTG4	SC70	DCK	5	250	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74AHC1G08DRLR	SOT-5X3	DRL	5	4000	180.0	9.5	1.78	1.78	0.69	4.0	8.0	Q3
SN74AHC1G08DRLR	SOT-5X3	DRL	5	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHC1G08DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
SN74AHC1G08DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
SN74AHC1G08DBVRG4	SOT-23	DBV	5	3000	180.0	180.0	18.0
SN74AHC1G08DBVTG4	SOT-23	DBV	5	250	180.0	180.0	18.0
SN74AHC1G08DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
SN74AHC1G08DCKR	SC70	DCK	5	3000	210.0	185.0	35.0
SN74AHC1G08DCKRG4	SC70	DCK	5	3000	180.0	180.0	18.0
SN74AHC1G08DCKTG4	SC70	DCK	5	250	180.0	180.0	18.0
SN74AHC1G08DRLR	SOT-5X3	DRL	5	4000	184.0	184.0	19.0
SN74AHC1G08DRLR	SOT-5X3	DRL	5	4000	202.0	201.0	28.0



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NOTES:

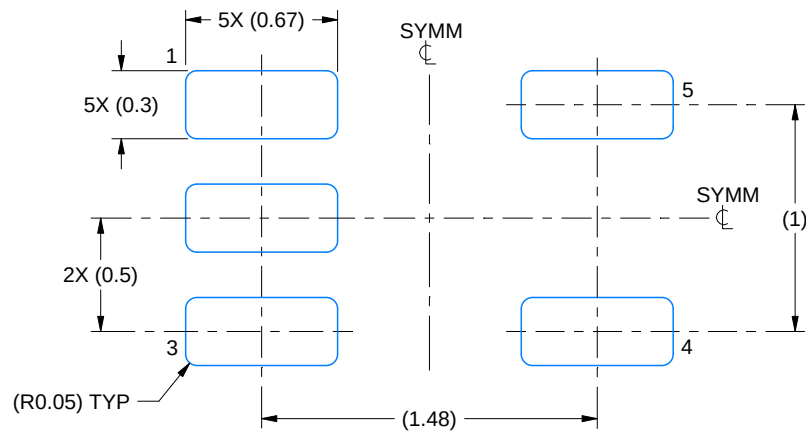
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-293 Variation UAAD-1

EXAMPLE BOARD LAYOUT

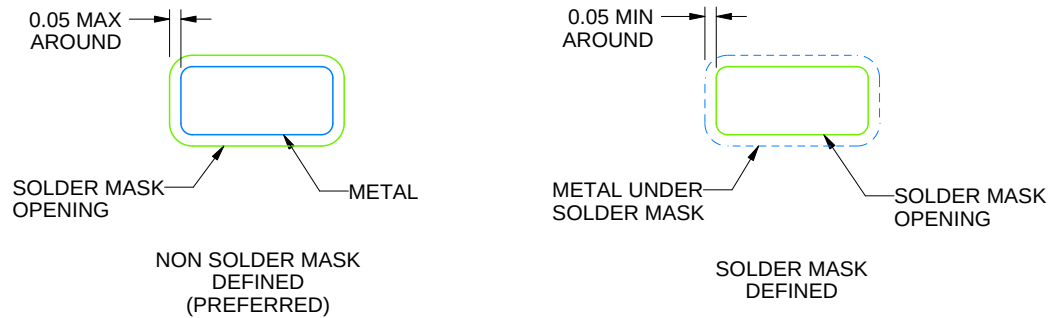
DRL0005A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
SCALE:30X



SOLDERMASK DETAILS

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NOTES: (continued)

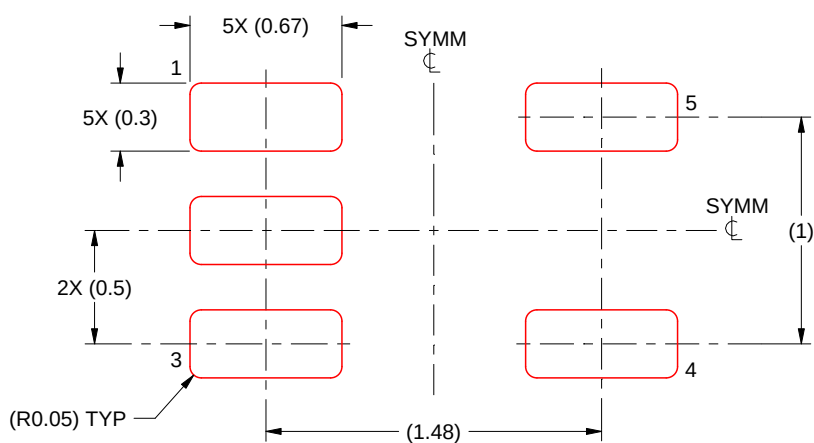
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DRL0005A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE

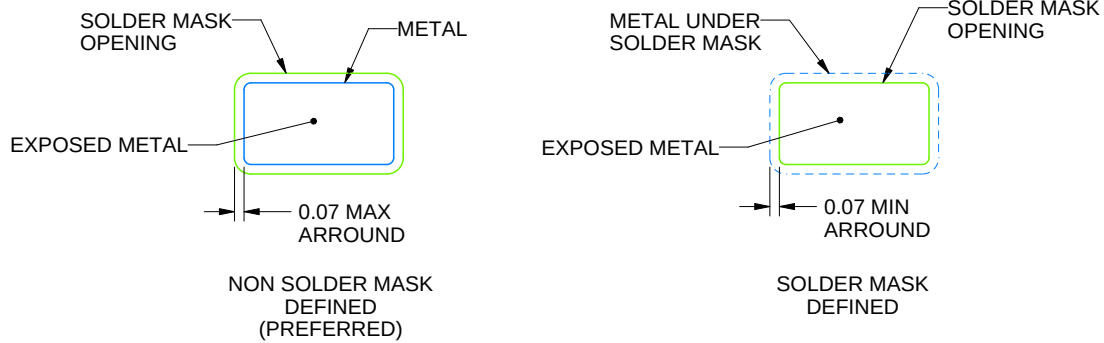
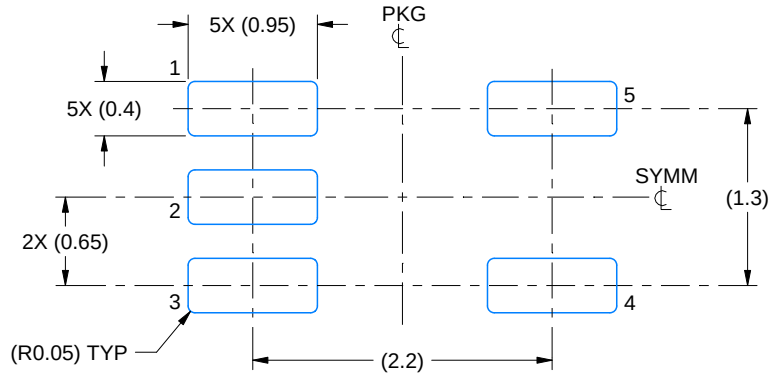


SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

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NOTES: (continued)

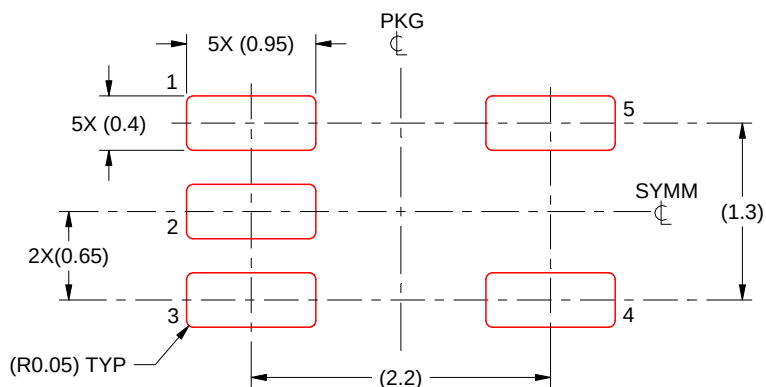
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.



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NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
 BASED ON 0.125 THICK STENCIL
 SCALE:18X

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NOTES: (continued)

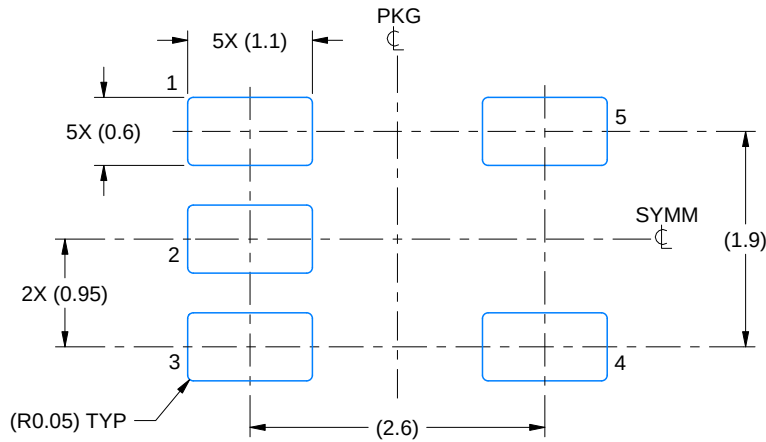
9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

EXAMPLE BOARD LAYOUT

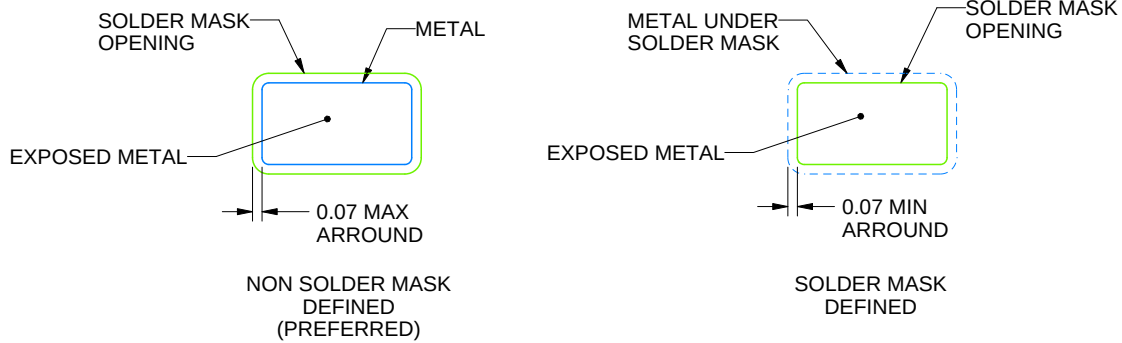
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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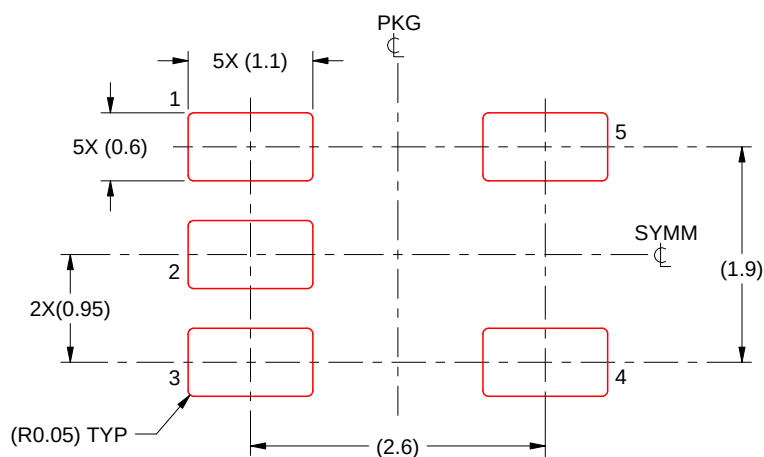
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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