MP6539

100V, Three-Phase, BLDC Motor Pre-Driver with HS & LS Inputs

The Future of Analog IC Technology

DESCRIPTION

The MP6539 is a gate driver IC designed for three-phase, brushless DC motor driver applications. The MP6539 is capable of driving three half-bridges consisting of six N-channel power MOSFETs up to 100V.

The MP6539 uses a bootstrap capacitor to generate a supply voltage for the high-side MOSFET driver. An internal charge pump maintains the high-side gate driver if the output is held high for an extended period of time.

Full protection features include programmable over-current protection (OCP), adjustable dead-time control, under-voltage lockout (UVLO), and thermal shutdown.

The MP6539 is available in TSSOP-28 (9.7mmx6.4mm) and QFN-28 (4mmx5mm) packages with an exposed thermal pad.

FEATURES

- Supports 100V Operation
- 120V V_{BST} Maximum Voltage
- Internal LDO Supports External NPN for High-Current Drive Requirements
- Integrated Current-Sense Amplifier
- Low-Power Sleep Mode for Battery-Powered Applications
- Programmable Over-Current Protection (OCP) for External MOSFETs
- Adjustable Dead-Time Control to Prevent Shoot-Through
- Thermal Shutdown and Under-Voltage Lockout (UVLO) Protection
- Fault Indication Output
- Available in Thermally Enhanced Surface-Mounted TSSOP and QFN Packages

APPLICATIONS

- Three-Phase Brushless DC Motors and Permanent Magnet Synchronous Motors
- Power Drills
- E-Bikes

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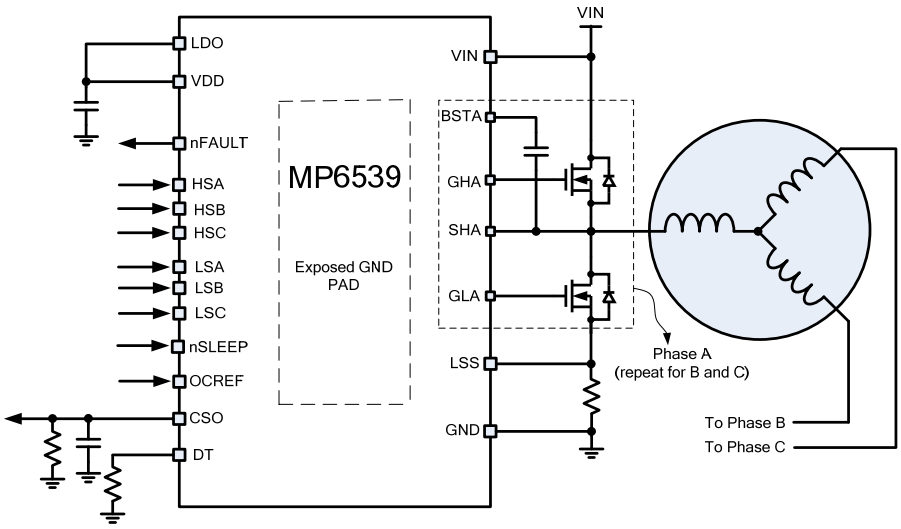
TYPICAL APPLICATION



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ORDERING INFORMATION

Part Number	Package	Top Marking
MP6539GV*	QFN-28 (4mm x 5mm)	*See Below*
MP6539GF**	TSSOP-28 EP	*See Below*

* For Tape & Reel, add suffix –Z (e.g.: MP6539GV–Z)
** For Tape & Reel, add suffix –Z (e.g.: MP6539GF–Z)

TOP MARKING (MP6539GV)

MPSYWW
MP6539
LLLLLL

MPS: MPS prefix
Y: Year code
WW: Week code
MP6539: Part number
LLLLLL: Lot number

TOP MARKING (MP6539GF)

MPSYYWW
MP6539
LLLLLLLLL

MPS: MPS prefix
YY: Year code
WW: Week code
MP6539: Part number
LLLLLLLLL: Lot number

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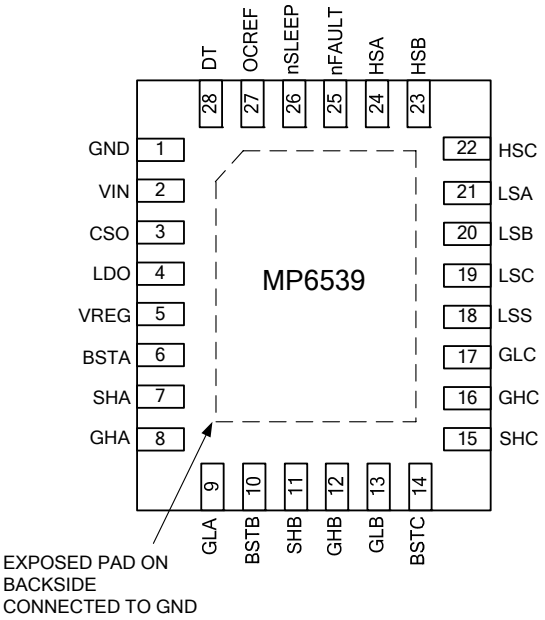
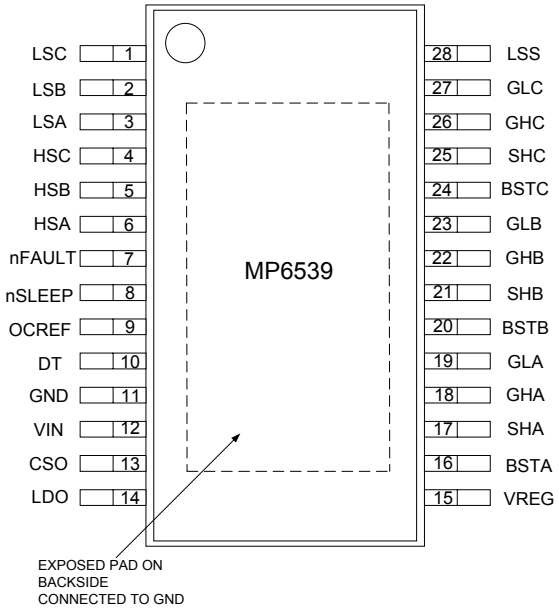
PACKAGE REFERENCE

TOP VIEW



QFN-28 (4mmx5mm)

TOP VIEW



TSSOP-28 EP

ABSOLUTE MAXIMUM RATINGS (1)

Input voltage (V_{IN}) ..... -0.3V to 110V
Input voltage VREG, GLA/B/C..... -0.3V to 14.5V
LDO ..... -0.3V to 14.5V
BSTA/B/C ..... -0.3V to 120V
GHA/B/C ..... -0.3V to (BST-SH) + 0.3V
GHA/B/C (transient, 2µs) .....
..... -8V to (BST-SH) + 0.3V
LSS ..... -0.3V to 4V
LSS (transient, 2µs) ..... -1V to 4V
SHA/B/C ..... -5V to 110V
SHA/B/C (transient, 2µs) ..... -8V to 110V
All other pins to GND ..... -0.3V to 6.5V
Continuous power dissipation (T_A = +25°C) **(2)**
QFN-28 (4mmx5mm) 3.1W
TSSOP-28 EP (9.7mmx6.4mm) 3.9W
Storage temperature ..... -55°C to +150°C
Junction temperature ..... +150°C
Lead temperature (solder) ..... +260°C

Recommended Operating Conditions (3)

Input voltage (V_{IN}) ..... +8V to 100V
Input voltage (V_{REG})..... +8.5V to 14V
OCREF voltage (V_{OC}) ..... 0.125V to 2.4V
Operating junction temp. (T_J)....-40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

	θ_{JA}	θ_{JC}
QFN-28 (4mmx5mm)	40	9 °C/W
TSSOP-28 EP	32	6 °C/W

NOTES:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 48V, VREG = 12V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Power Supply						
Input supply voltage	V_{IN}		8		100	V
LDO output voltage	V_{LDO}	$I_{LDO} \leqslant$ 5mA, V_{IN} > 15V	10.8	12	13.2	V
Gate driver supply voltage	V_{REG}		8.5		14	V
Quiescent current	I_Q	nSLEEP = 1, not switching		0.7		mA
	I_{SLEEP}	nSLEEP = 0			1	µA
Control Logic						
Input logic low threshold	V_{IL}				0.8	V
Input logic high threshold	V_{IH}		2			V
Logic input current	$I_{IN(H)}$	V_{IH} = 0.8V	-2.4		2.4	µA
	$I_{IN(L)}$	V_{IL} = 5V	-14		14	µA
nSLEEP pull-down resistance	$R_{SLEEP-PD}$			450		kΩ
Internal pull down resistance	R_{PD}			450		kΩ
Fault Output (Open-Drain Output)						
Output low voltage	V_{OL}	I_O = 5mA			0.1	V
Output high leakage current	I_{OH}	V_O = 3.3V			1	µA
Protection Circuit						
V_{REG} UVLO rising threshold	V_{REG_RUVLO}		6.5	7.5	8.5	V
V_{REG} UVLO falling threshold	V_{REG_FUVLO}		6	6.8	7.6	V
V_{REG} UVLO hysteresis	V_{REG_HYS}			610		mV
V_{IN} UVLO rising threshold	V_{VIN_RUVLO}		3.6	4	4.4	V
V_{IN} UVLO falling threshold	V_{VIN_FUVLO}		3.4	3.8	4.3	V
V_{IN} UVLO hysteresis	V_{VIN_HYS}			100		mV
V_{BST} UVLO threshold	V_{BST_UVLO}	Voltage between SHx and BSTx		4		V
OCREF threshold	V_{OC}	V_{OC} = 1V	0.8	1	1.2	V
		V_{OC} = 2.4V	2.18	2.4	2.62	V
OCP deglitch time	t_{OC}			2.7		µs
Sleep wake-up time	t_{SLEEP}			2		ms
Thermal shutdown	T_{TSD} (5)			175		°C
Thermal shutdown hysteresis	T_{TSD_HYS} (5)			20		°C
Gate Drive						
Bootstrap diode forward voltage	V_{FBOOT}	I_D = 10mA			1.2	V
		I_D = 50mA			2.3	V
Maximum source current	DS_O (5)			0.8		A
Maximum sink current	DS_I (5)			1		A
Gate drive pull-up resistance	R_{UP}	V_{DS} = 1V		7		Ω
HS gate drive pull-down resistance	R_{HS-DN}	V_{DS} = 1V	0.6		4.5	Ω
LS gate drive pull-down resistance	R_{LS-DN}	V_{DS} = 1V	0.6		4.5	Ω
LS automatic turn-on time	t_{LS}			4.6		µs
Dead time	t_{DEAD}	R_{DT} = 10kΩ		560		ns
		R_{DT} = 100kΩ		4.5		µs
		DT tied to GND		77		ns

NOTE:

5) Guaranteed by design.

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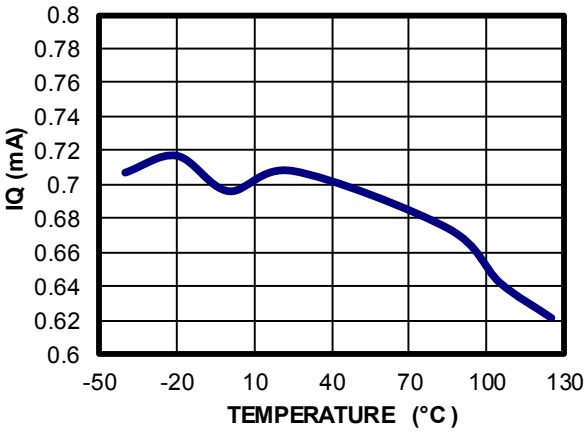
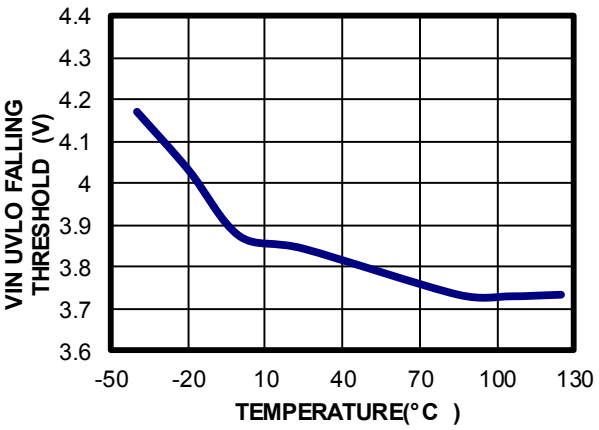
TYPICAL CHARACTERISTICS

V_{IN} = 48V, unless otherwise noted.

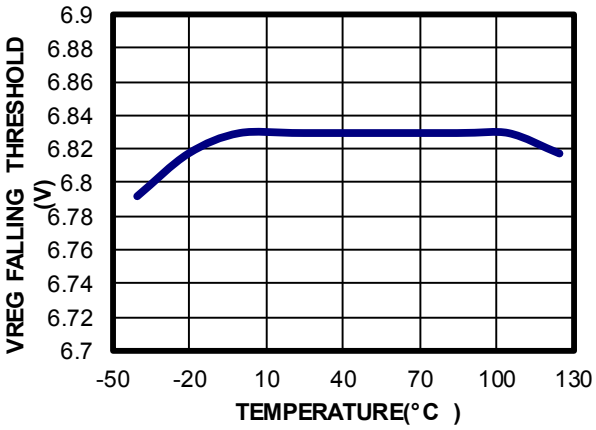
Quiescent Current vs. Temperature



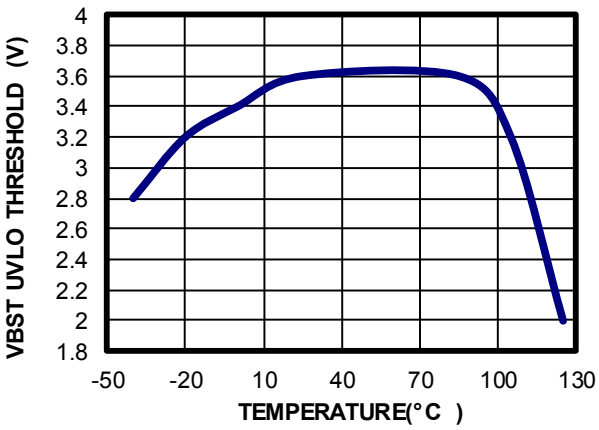
V_{IN} UVLO Falling Threshold vs. Temperature



V_{REG} Falling Threshold vs. Temperature

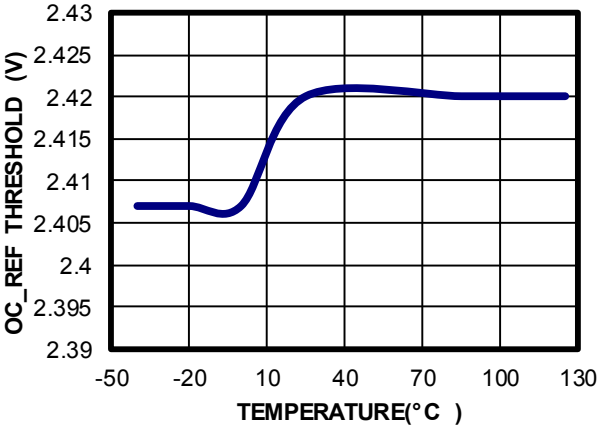


V_{BST} UVLO Threshold vs. Temperature

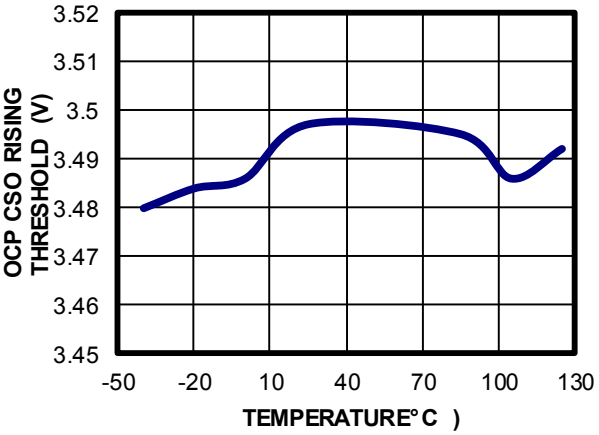


OCREF Threshold vs. Temperature

OCREF = 2.4V



OCP CSO Rising Threshold vs. Temperature



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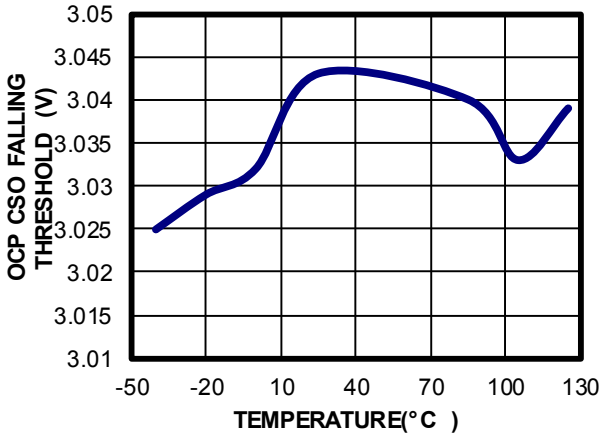
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 48V, unless otherwise noted.

OCP CSO Falling Threshold vs. Temperature



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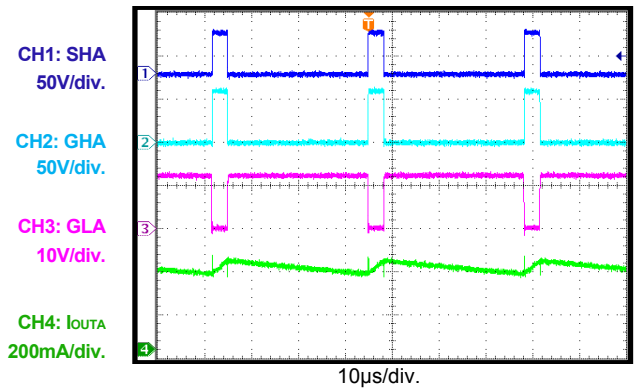
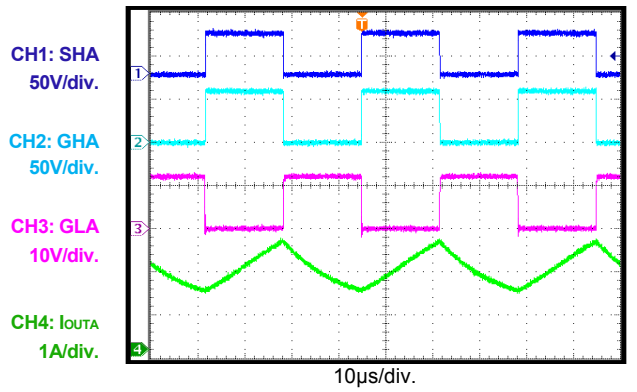
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 48V, OCREF = 0.5V, R_{DT} = 1kΩ, A phase switching, B phase LS on, f_{PWMA} = 30kHz, T_A = 25°C, resistor + inductor load: 5Ω + 1mH/phase with star connection, unless otherwise noted.

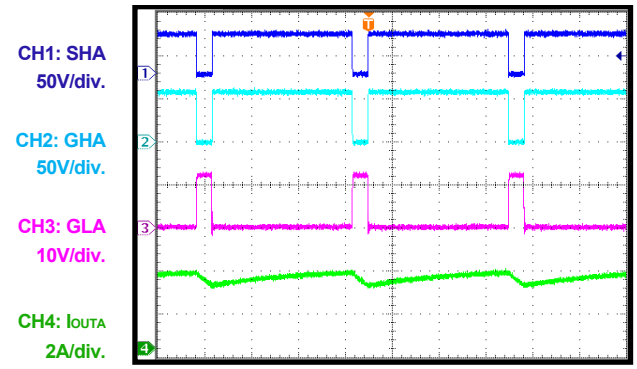
Steady State
Duty = 10%



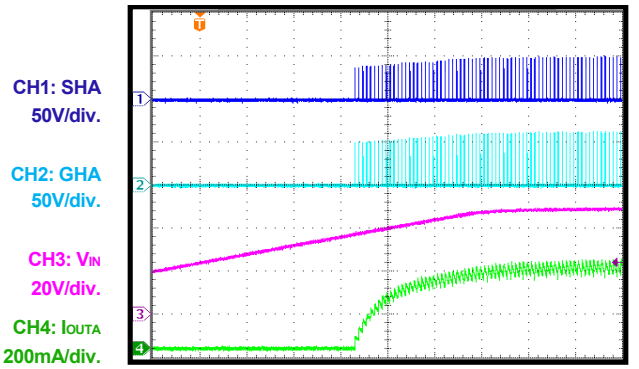
Steady State
Duty = 50%



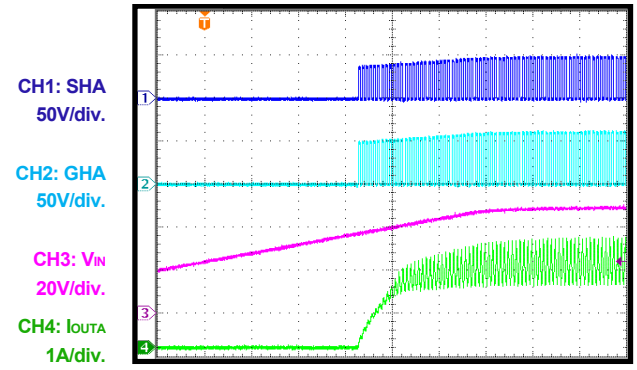
Steady State
Duty = 90%



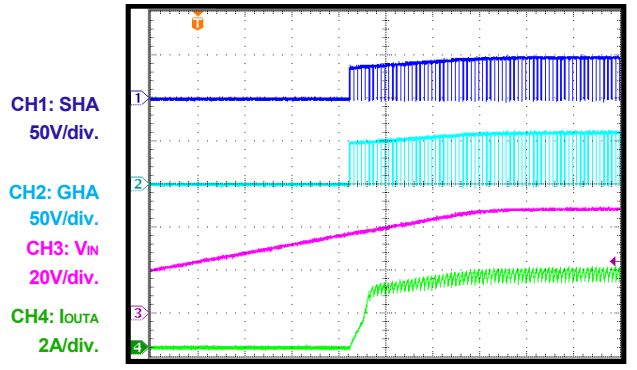
Power Ramp-Up
Duty = 10%



Power Ramp-Up
Duty = 50%



Power Ramp-Up
Duty = 90%



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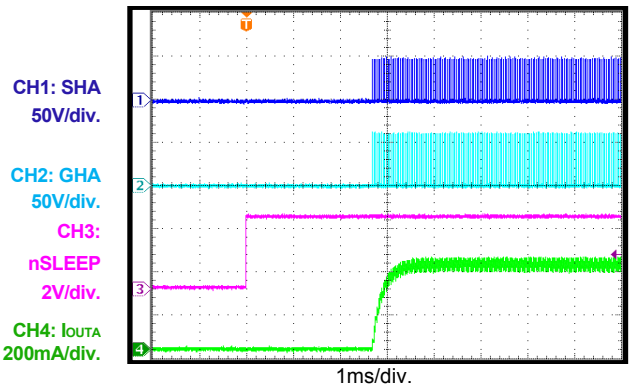
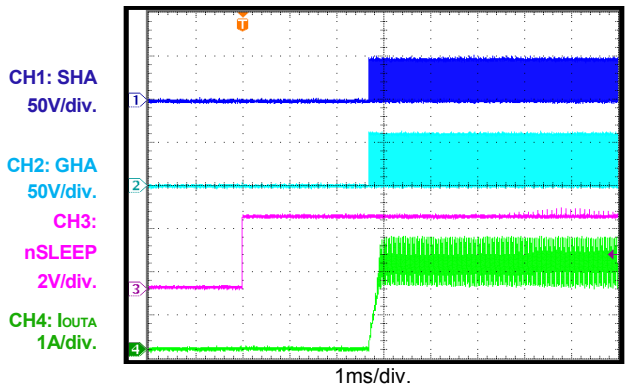
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 48V, OCREF = 0.5V, R_{DT} = 1kΩ, A phase switching, B phase LS on, f_{PWMA} = 30kHz, T_A = 25°C, resistor + inductor load: 5Ω + 1mH/phase with star connection, unless otherwise noted.

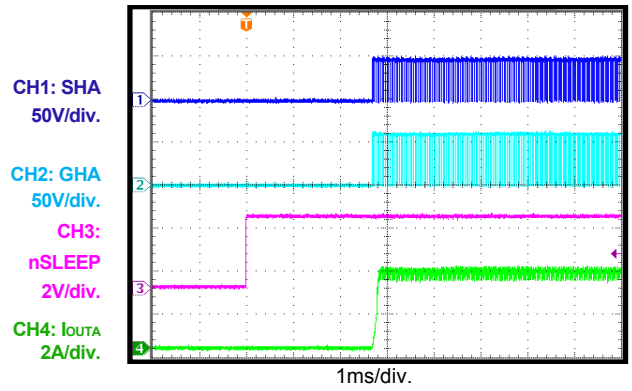
Sleep Recovery
Duty = 10%



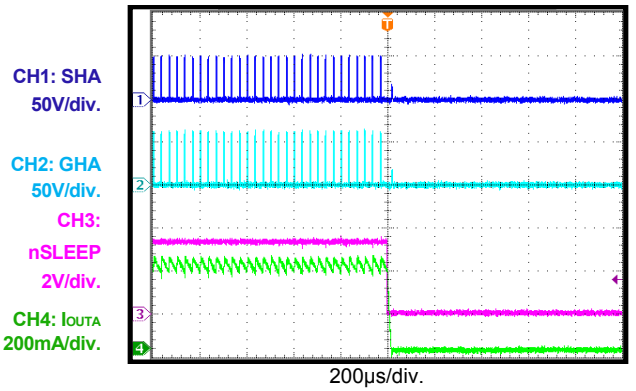
Sleep Recovery
Duty = 50%



Sleep Recovery
Duty = 90%



Sleep Entry
Duty = 10%



Sleep Entry
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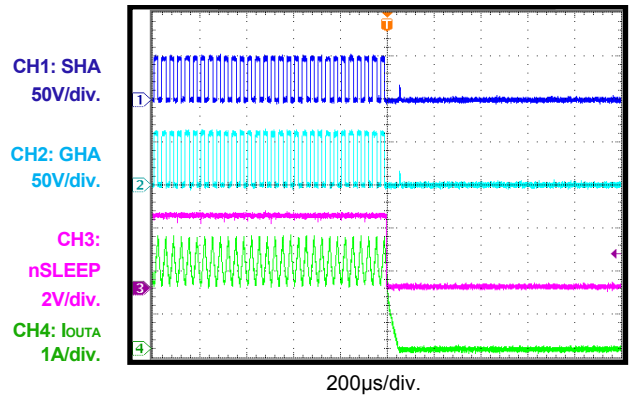

Sleep Entry
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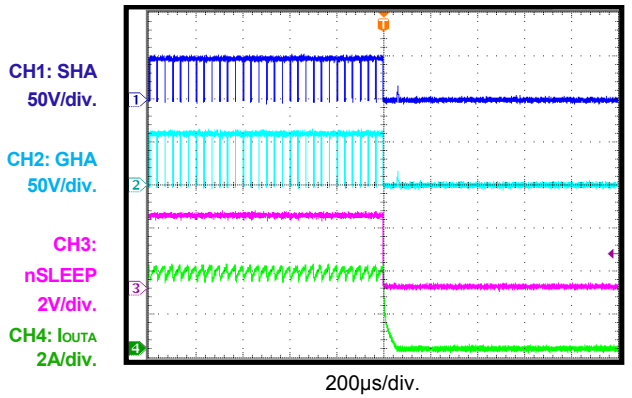

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PIN FUNCTIONS

QFN-28 Pin #	TSSOP Pin #	Name	Description
1	11	GND	**Ground.**
2	12	VIN	**Input supply voltage.**
3	13	CSO	**Current sense output and OCP off time adjust.**
4	14	LDO	**Gate drive LDO output/base drive for external NPN transistor.**
5	15	VREG	**Gate driver supply voltage.**
6	16	BSTA	**Bootstrap output phase A.**
7	17	SHA	**High-side source connection phase A.**
8	18	GHA	**High-side gate drive phase A.**
9	19	GLA	**Low-side gate drive phase A.**
10	20	BSTB	**Bootstrap output phase B.**
11	21	SHB	**High-side source connection phase B.**
12	22	GHB	**High-side gate drive phase B.**
13	23	GLB	**Low-side gate drive phase B.**
14	24	BSTC	**Bootstrap output phase C.**
15	25	SHC	**High-side source connection phase C.**
16	26	GHC	**High-side gate drive phase C.**
17	27	GLC	**Low-side gate drive phase C.**
18	28	LSS	**Low-side source connection.**
19	1	LSC	**Phase C low-side input pin.**
20	2	LSB	**Phase B low-side input pin.**
21	3	LSA	**Phase A low-side input pin.**
22	4	HSC	**Phase C high-side input pin.**
23	5	HSB	**Phase B high-side input pin.**
24	6	HSA	**Phase A high-side input pin.**
25	7	nFAULT	**Fault indication.** nFAULT is an open-drain output type. nFAULT is logic low when in a fault condition.
26	8	nSLEEP	**Sleep mode input.** Logic low to enter low-power sleep mode; high to enable. Internal pulldown.
27	9	OCREF	**Over-current protection reference input.**
28	10	DT	**Dead time setting.**

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BLOCK DIAGRAM

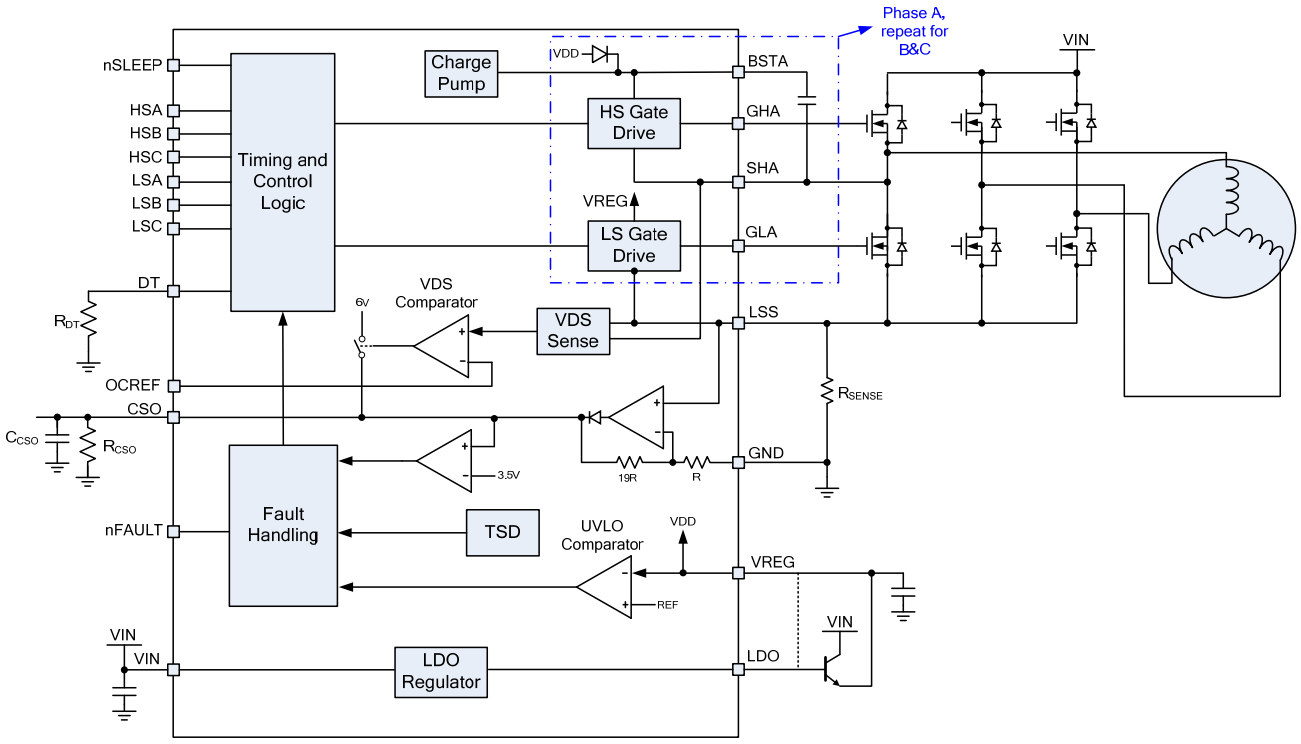

Figure 1: Functional Block Diagram

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OPERATION

The MP6539 is a three-phase, BLDC motor pre-driver that can drive three half-bridges with a 0.8A source and 1A sink current capability. The MP6539 supports operation up to 100V. The MP6539 features a low-power sleep mode, which disables the device and draws very low supply current.

The MP6539 provides several flexible functions, such as adjustable dead-time control and over-current protection (OCP), which allow the device to cover a wide range of applications.

Power-Up Sequence

The power-up sequence is initiated by the application of voltage to VIN and the voltage present on VREG. Usually, VREG is supplied by an internal LDO regulator connected to VIN, but it is also possible to drive VREG from another power source.

To initiate a power-up, VIN must be above ~4.5V, and VREG must be above the VREG under-voltage lockout (UVLO) threshold of 7.4V. If VREG is supplied by the internal LDO regulator, this means that VIN must be at about 8V before the part starts to power up. After VREG exceeds the VREG UVLO threshold, the MP6539 sequentially turns on each low-side MOSFET (LS-FET) in succession to charge the bootstrap capacitors.

The power-up process takes between 1ms and 2ms, after which the MP6539 responds to logic inputs and drives the outputs.

Input Logic

Driving nSLEEP low puts the device into a low-power sleep state. In this state, all internal circuits are disabled. All inputs are ignored when nSLEEP is active low. When waking up from sleep mode, approximately 1ms of time must pass before issuing a pulse-width modulation (PWM) command to allow the internal circuitry time to stabilize.

HSx is used to control the gate driver for the high-side MOSFET (HS-FET) of each phase. LSx is used to control the gate driver for the LS-FET. A positive dead time is enforced by the device. If both HSx and LSx are driven high, neither MOSFET is driven (see Table 1).

Table 1: Input Logic Truth Table

LSx	HSx	SHx
H	H	High impedance
H	L	GND
L	H	VIN
L	L	High impedance

nFAULT

nFAULT reports to the system when a fault condition occurs, such as over-current protection (OCP) or over-temperature protection (OTP). nFAULT is an open-drain output type and is driven low when a fault condition occurs. If the fault condition is released, nFAULT is pulled up to a high level by an external pull-up resistor.

Current-Sense Amplifier

An integrated current-sense amplifier amplifies the voltage on LSS (relative to GND) by a factor of 20. This voltage is the output to CSO.

The current-sense amplifier only sources current. An external capacitor of 1nF (minimum) must be connected from CSO to ground for stability.

During the PWM on time, current flowing through the output MOSFETs also flows through the shared low-side current sense resistor, generating a voltage that is amplified by the current-sense amplifier, which charges the external capacitor on CSO. During the PWM off time, current recirculates through the LS-FETs and does not pass through the sense resistor, so there is zero voltage across it. During this time, the capacitor discharges through the internal feedback resistor (approximately 450kΩ) and also through any external resistor to ground. Select an external resistor and capacitor to provide a filter to hold the value of the current through the PWM off time. Any external resistor used should be 1kΩ or larger.

Over-Current Protection (OCP) / Current Regulation

The voltage across each LS-FET is monitored by a comparator in the MP6539 to turn the device off in the event of an over-current condition. The over-current shutdown voltage threshold level is programmable through OCREF by applying an external reference voltage with a DAC or resistor divider. When

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the VDS of the MOSFET exceeds OCREF, CSO is pulled to ~6V internally. Whenever CSO exceeds 3.5V, an OCP event is detected, and all output MOSFETs are turned off. nFAULT is driven active low.

Once the current through the LS-FETs and the sense resistor stops, the CSO voltage is no longer driven and starts to fall at a rate determined by the external capacitor and resistor. When the voltage falls below 2.9V, the output MOSFETs are re-enabled, and nFAULT is inactive.

The resulting off time is set by the value of the external capacitor and the internal feedback resistor in parallel with the external resistor (if used).

The off time generated when CSO reaches 3.5V can be approximated with Equation (1):

$$t_{OFF}\,(\mu s) = 0.2*R(k\Omega)*C(nF) \quad (1)$$

The off time generated when VDS exceeds OCREF is longer since CSO is pulled to 6V and must decay to 2.9V for the outputs to be re-enabled. This off time can be approximated with Equation (2):

$$t_{OFF}\,(\mu s) = 0.6*R(k\Omega)*C(nF) \quad (2)$$

Where C is the capacitance from CSO to ground, and R is the total resistance from CSO to ground, comprised of the internal feedback resistor (~450kΩ) in parallel with any external resistor to ground.

This feature can be used for current regulation to limit the stall/start-up current of a motor, either by using an external current sense resistor or (with lower accuracy) the $R_{DS(ON)}$ of the LS-FET.

In addition to low-side current monitoring, a circuit monitors the output and triggers a fault condition of the output, driving it high, but it will not rise above ~4.5V. This provides protection against a short to ground, which would not be detected by low-side current sensing. If this occurs, the MP6539 enters a latched fault state and disables all outputs. The MP6539 remains latched off until it is reset by nSLEEP or UVLO.

Gate-Drive Voltage Regulator

To generate a voltage to drive the external MOSFET gates, a linear regulator is integrated into the MP6539.

If current over about 5mA is needed (to drive the high gate charge MOSFETs at a high switching frequency), an external NPN transistor (and optionally also a resistor) must be used to remove power dissipation from the IC.

For low-current applications, LDO is connected to VREG directly. For higher current requirements, an NPN transistor is used (see Figure 2).

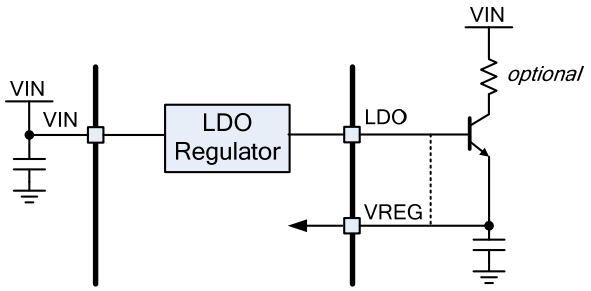

Figure 2: High-Current Configuration of the LDO

If desired, an appropriate gate-drive supply voltage can be supplied directly to VREG from an external supply. In this case, connect only the capacitor to LDO. VIN must still be connected to the motor supply voltage.

OCP Deglitch Time

There is usually a current spike during the switching transition due to the body diode's reverse-recovery current or the distributed inductance or capacitance. This current spike requires filtering to prevent it from erroneously triggering OCP and shutting down the external MOSFET. An internal, fixed, deglitch time (t_{OC}) (which is also the minimum on time for the MOSFET) blanks the output of the VDS monitor when the outputs are switched.

Charge Pump and Bootstrap

Normally, the high-side gate-drive voltage is generated from bootstrap capacitors connected between SHx and BSTx. The bootstrap capacitor is charged whenever the LS-FET is turned on.

If the output is held at a high state for a long period of time, the bootstrap capacitor

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discharges slowly. This eventually results in gate driver loss for the HS-FET.

To prevent this, an internal charge pump generates a voltage to maintain the bootstrap capacitor charge.

The bootstrap voltage is monitored by an under-voltage detection circuit. If any bootstrap voltage falls below the VBST UVLO voltage, the part initiates a new power-up sequence.

Dead-Time Adjustment

To prevent shoot-through in any phase of the bridge, it is necessary to insert a dead time (t_{DEAD}) between a high- or low-side turn-off and the next complementary turn-on event. The dead time for all three phases is set by a single dead-time resistor (R_{DT}) between DT and ground using Equation (3):

$$t_{DEAD}(\mu s) = 0.044*R(k\Omega) + 0.1 \quad (3)$$

If DT is tied to GND directly, an internal minimum dead time of 30ns is applied. Leave DT open to generate a 6μs dead time.

VREG and VIN UVLO Protection

If at any time the voltage on VREG falls below the VREG UVLO threshold voltage, the outputs are disabled, and the nFAULT signal is asserted. Operation resumes with a bootstrap refresh when VREG rises above the UVLO threshold.

If the voltage on VIN falls below the VIN UVLO threshold voltage, all circuitry in the device is disabled, and the internal logic is reset. nFAULT is not asserted. Operation resumes when VREG rises above the UVLO threshold.

Thermal Shutdown

If the die temperature exceeds safe limits, the MP6539 enters a latched fault state similar to an OCP event, and nFAULT is driven low. Only nSLEEP or UVLO can unlatch the device from an OTP fault lockout.

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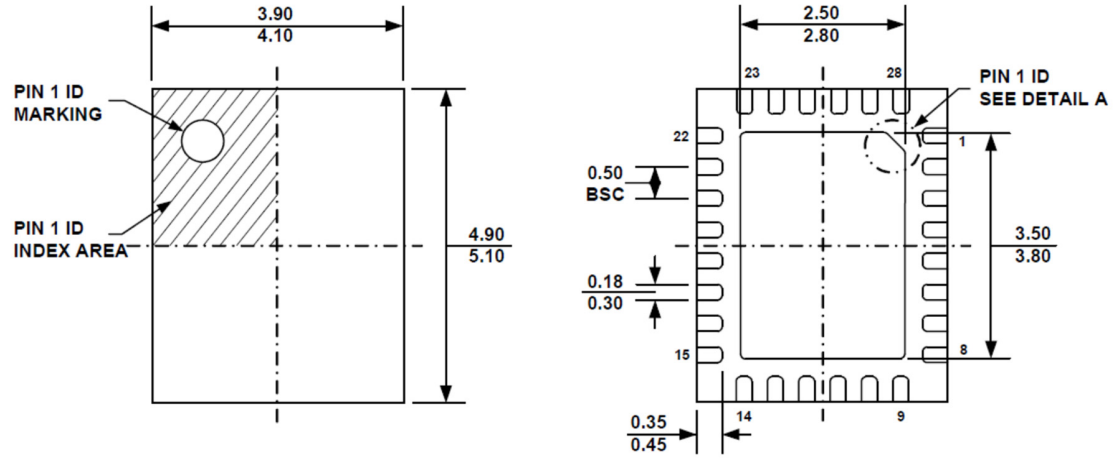
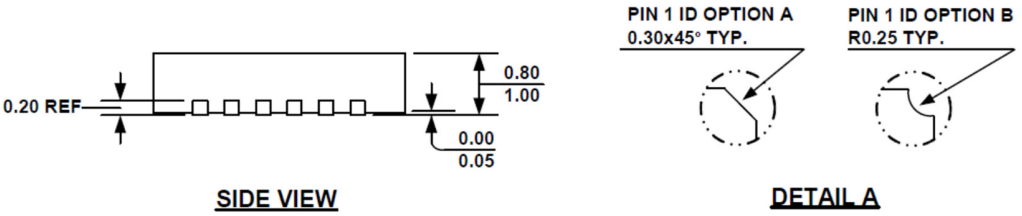
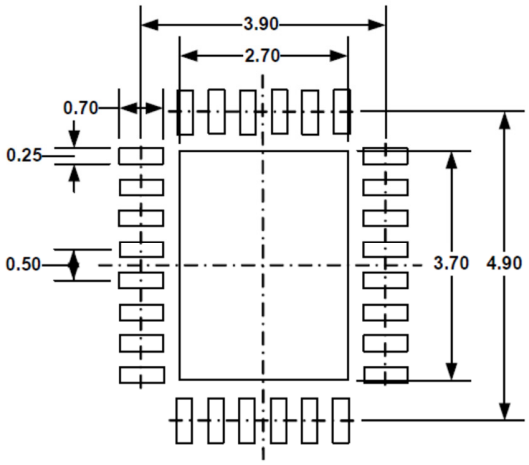
PACKAGE INFORMATION

QFN-28 (4mmx5mm)







NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETER MAX.
4) DRAWING CONFORMS TO JEDEC MO-220, VARIATION VHGD-3.
5) DRAWING IS NOT TO SCALE.

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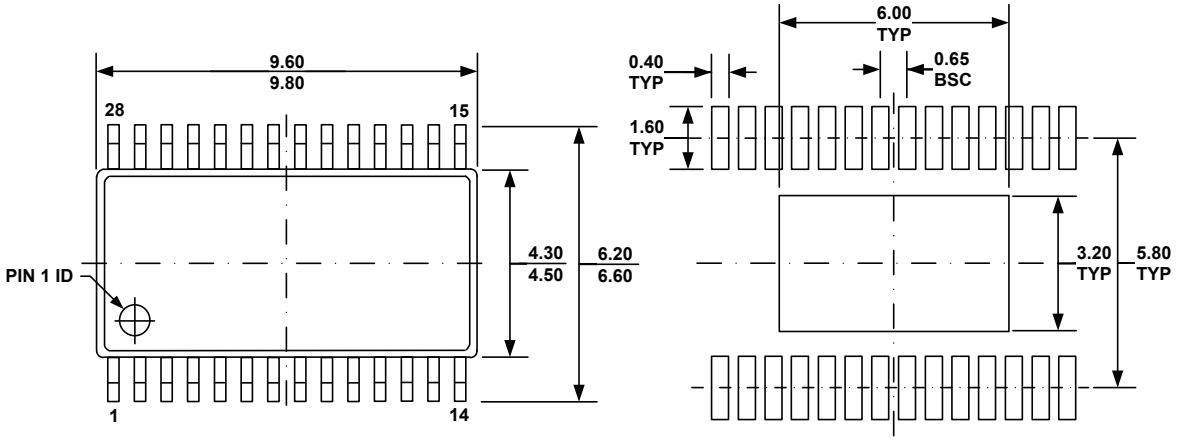
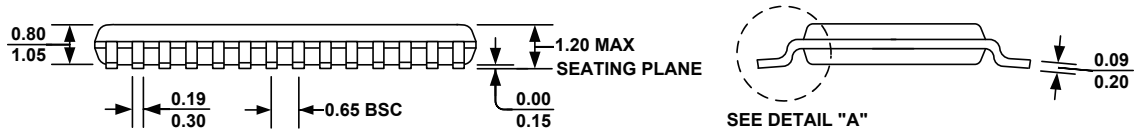
PACKAGE INFORMATION *(continued)*

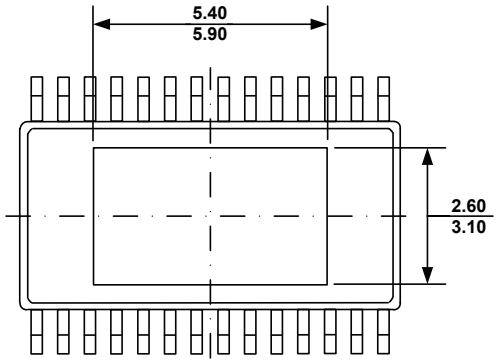
TSSOP-28 EP



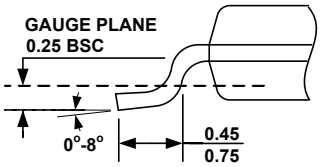
TOP VIEW **RECOMMENDED LAND PATTERN**



FRONT VIEW **SIDE VIEW**



BOTTOM VIEW



DETAIL "A"

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) DRAWING CONFORMS TO JEDEC MO-153, VARIATION AET.
6) DRAWING IS NOT TO SCALE.

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